WHAT IS CLAIMED IS:

1. A memory control apparatus which performs a reading operation on a memory device at a request of a plurality of masters, comprising:

read means for pre-reading data subsequent to data which any of the plurality of masters requests to read;

a prefetch buffer for holding a result of the pre-reading;

set means for setting a specific master among the plurality of masters; and

control means for determining whether or not the master which issues the request is a master set by said set means when the read request is issued from any of the plurality of masters, and storing a result of the pre-reading in said prefetch buffer when it is determined that the master which issues the request is a master set by said set means.

2. The memory control apparatus according to claim 1, wherein

said set means can arbitrarily set the specific master among the plurality of masters.

3. The memory control apparatus according to claim 1, wherein

said apparatus is connected to the plurality of

masters through a shared bus.

4. The memory control apparatus according to claim 1, wherein

said read means simultaneously pre-reads data and reads data requested by the master.

5. The memory control apparatus according to claim 1, wherein

said read means simultaneously reads data requested by the master and pre-reads data subsequent to the requested data.

6. The memory control apparatus according to claim 5, wherein

said prefetch buffer stores data requested by the master and data subsequent to the requested data.

7. The memory control apparatus according to claim 1, wherein

said prefetch buffer stores one or more sets of information including data, an address of the data, and a flag indicating the validity of the data.

8. The memory control apparatus according to claim 7, wherein

when the master requests a read, said control

means compares a requested address with an address of data stored in said prefetch buffer, checks a flag of the data, returns the data as read data of the master when the addresses match each other, and the flag is a valid flag, and stores a result of the pre-read in said prefetch buffer when there is no matching data, and the master is set by said set means.

9. The memory control apparatus according to claim 7, wherein

when the master requests a write, a requested address is compared with an address of data stored in said prefetch buffer, and the flag is changed into a nullified state as necessary.

10. The memory control apparatus according to claim 7, wherein

when the master requests a write, a requested address is compared with an address of data stored in said prefetch buffer, and data stored in said prefetch buffer is replaced as necessary with data to be written.

11. The memory control apparatus according to claim 1, wherein

said set means can set a plurality of specific masters.